Register No : _____

THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)

UG/PG DEGREE END SEMESTER THEORY EXAMINATIONS, APRIL-MAY 2026

Third Semester

Computer Science and Engineering

UECTL24302 - DIGITAL PRINCIPLES AND COMPUTER ORGANIZATION

(Common to AIDS & IT Departments)

Regulations - 2024

Duration : 3 Hrs ***Maximum : 100 Marks***

PART – A (ANSWER ALL QUESTIONS) (Marks 10*2=20)

Q.No	Questions	BTL	CO	Marks
1.	Design a magnitude comparator that compares two one bit numbers.	L2	1	2
2.	Explain the purpose of valid pin in Encoder.	L2	1	2
3.	Distinguish between the Mealy and Moore Models of sequential circuits.	L2	2	2
4.	Explain ripple counter with an example.	L2	2	2
5.	Specify the purpose of PC in a processor.	L2	3	2
6.	Explain the need for encoding of machine instructions.	L2	3	2
7.	Identify the hazard that causes delay in the execution of the following program. Add R2, R3, #100 Subtract R9, R2, #30	L3	4	2
8.	Differentiate between hardwired and microprogrammed control units.	L2	4	2
9.	List the purpose of Translation Lookaside Buffer.	L2	5	2
10.	Estimate the average access time when cache hit rate is 0.9 and time to access from cache memory and main memory are 2 cycle and 9 cycles respectively.	L3	5	2

PART – B (ANSWER ALL QUESTIONS) (Marks 5*16 = 80)

Q.No			Questions	BLT	CO	Marks
11.	a	i	Simplify the following Boolean expression to Sum of product and Product of sum using Karnaugh map F(A,B,C.D)= A ' B ' + A C D ' + A B C + A ' B ' C D ' + B' D	L3	1	8
		ii	Design a full subtractor and write the HDL code for the same circuit.	L2	1	8
			Or			
	b	i	Design a 5 x 32 decoder by using 3 x 8 decoders and a 2 x 4 decoder.	L2	1	8
		ii	An 8X1 multiplexer has inputs A, B and C connected to the selection inputs S_2, S_1 and S_0, respectively. The data inputs I_0 through I_7 are as follows: $I_1 = I_2 = I_7 = 0$; $I_3 = I_5 = 1$; $I_0 = I_4 = D$ and $I_6 = D'$. Determine the Boolean function that the multiplexer implements.	L3	1	8
12.	a		A sequential circuit with two D flip-flops, A and B; two inputs, x and y; and one output, z, is specified by the following next state and output equations: A(t+1) = x'y + xA B(t+1) = x'B + xA z=B (i) Draw the logic diagram of the circuit (ii) List the state table for the sequential circuit (iii) Draw the corresponding state diagram	L2	2	16
			Or			
	b		Design 4 bit counter using flip-flops and also discuss how the counter can be modified to implement Johnson Counter.	L2	2	16

13.	a	i	Illustrate the function units of a computer with neat diagram.	L2	3	8
		ii	Summarize the factors that need to be considered while designing the Instruction Set Architecture (ISA) of a processor.	L2	3	8
			Or			
	b		Explain the addressing modes in detail with suitable examples. Provide a brief description of each addressing mode and its purpose.	L2	3	16
14.	a	i	Classify the different types of hazards, illustrate each with suitable examples, and evaluate the techniques used to handle or mitigate these hazards.	L2	4	8
		ii	Develop the control sequence required for execution of instruction ADD ADDR, R2, #DATA, where the format is ADD dst,src1,src2 and explain the single bus organization of datapath with a neat diagram.	L2	4	8
			Or			
	b	i	Explain the process of generating control signals using a hardwired control unit and highlight its key advantages.	L2	4	8
		ii	Design a microprogram to outline, specify, and sequence the actions required to fetch and execute the instruction ADD $(R_{src})+$, R_{dst}.	L2	4	8
15.	a	i	Explain virtual memory organization and the translation of virtual address into physical address.	L2	5	8
		ii	Explain the cache mapping methods used for cache block replacement.	L2	5	8
			Or			
	b	i	Illustrate the sequence of operations involved in a typical DMA transfer cycle. Include details about request initiation, data transfer, and completion using a state diagram.	L2	5	8
		ii	Explain interrupt I/O in details.	L2	5	8

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